1. (Proposed Amendment) A method to prevent starvation in a switched system comprising a distributed bus arbiter that varies a time between a request for the switched system resources as a function of a number of requests the system indicates to be retried, wherein the step of varying the time in the switched system is a function of a plurality of requests, but the method does not keep track of latency times of any selected processor.

2. The method of Claim 1 further comprising the bus arbiter first increasing the time between requests until the system no longer indicates to retry the request and the bus arbiter then decreasing the time between requests after a number of requests processed without the system indicating to retry any requests.

3. A method for preventing starvation in a switched system with a distributed bus arbiter, the method comprising:

a) the bus arbiter increasing a time between a request from a microprocessor connected to the switched system to use resources of a switch until the switch can process the request; and

b) the bus arbiter decreasing the time between the requests from the microprocessors connected to the switched system to use resources of the switch as a function of some number of requests processed without the bus arbiter having to increase the time between requests from the microprocessors connected to the switched system, wherein the steps of increasing or decreasing the time in the switched system is a function of a plurality of requests, but the method does not keep track of latency times of any selected processor.

4. A method for avoiding livelocks in a switched system with a distributed bus arbiter, whereby bus request logic varies a time between requests for resources of the switched system as a function of switch retries, the method comprising:

a) defining a first parameter that specifies a number of bus clocks to wait between requests from a microprocessor connected to the switched system;

b) defining a second parameter that specifies a number of sequential responses to be received from a system switch indicating it has a sufficient number of resources to process the request issued from the microprocessor connected the switched system;

c) issuing at least one request from the microprocessor to the system switch;

d) responsive to a signal from the system switch indicating it lacks resources to process a command, increasing the number of bus clocks to wait between issuance of requests from microprocessors by the number of bus clocks defined as the first parameter;

e) waiting the increased number of bus clocks between issuance of requests to the switch;

f) responsive to a signal from the system switch indicating it has resources to process a command, increasing a counter counting the number of signals from the system switch indicating it has resources to process a command;

g) responsive to a signal from the system switch indicating it lacks resources to process a command, resetting the value in the counter to zero;

h) comparing the value in the counter to the second parameter; and when the value in the counter is equal to the value of the second parameter, decreasing the number of bus clocks between issuance of requests to the switch from microprocessors connected to the switched system by the amount equal to the number of bus clocks defined as the first parameter and resetting the value in the counter to zero, wherein the steps of increasing or decreasing the time in the switched system is a function of a plurality of requests, but the method does not keep track of latency times of any selected processor.

5. The method of Claim 4 wherein the first parameter is defined at system power-on.

6. The method of Claim 4 wherein the second parameter is defined at system power-on.